



Original Contribution

**A 0.7-V, 1.9MW INTEGRATOR BASED ON SELF-BIASED DIGITAL INVERTER
IN 90NM CMOS TECHNOLOGY**

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ABSTRACT

This paper proposes a switched-capacitor integrator based on a self-biased digital inverter. By using the self-biasing technique, the gain performance of the integrator is improved and increased the power efficiency. The integrator is designed by employing standard CMOS 90nm technology. All transistors are operated within the supply voltage 0.7 V. The designed integrator is simulated in an input signal bandwidth of 8 KHz with a sampling frequency of 1.6 MHz. The integrator core consumes only 21nW of power and the total power consumption is 1.9mW. The proposed switched-capacitor integrator attains low power, low voltage and high speed performances for practical applications.

Key words: Switched-capacitor integrator; Self-biased digital inverter; Low power; High speed

INTRODUCTION

The most common approach to design an analog/mixed-signal circuit is using switched-capacitor in order to have discrete time signal processing. Switched-capacitor circuits include operational amplifier (op-amps), switches, and capacitors. One application of switched-capacitor circuits is in integrators. The basic element in the switched-capacitor integrator circuits is an operational transconductance amplifier (OTA) which consumes the most power in these circuits, but it is hard to design low voltage and low power OTAs in scaled CMOS technologies. Several techniques have been suggested to design low voltage analog circuits by using charge pumps (1), (2) switched-op amps (3), switched-RC (4) and the input-feed forward architecture (5). In charge pumps technique, higher voltage than the supply voltage is developed for switches (1), (2). Switched op-amps technique with common mode level shift is proposed to eliminate the need for charge pumps (3).

Switched-RC technique which achieves high linearity and low voltage operation are used in (4)

to make trade-off between speed and accuracy in switched op-amps circuits.

All mentioned approaches require extra control circuits and extra current with consumes high power and occupy the large area. In (5) are proposed the Ultra-deep-submicron standard digital CMOS technologies to minimize the power consumption in a low voltage environment. Also the input feed-forward architecture with the low power operational transconductance amplifier (OTA) is developed in (6). The supply voltages of the OTAs are confined and have reached the limits of further scaling. Thus, inverter-based amplifiers and self-biased fully differential super inverter has been reported recently (7), (8) in order to eliminate the OTAs requirement. The reason of using an inverter instead of amplifiers is its simplicity and the capability of operating with ultra-low supply voltages. Therefore, the single-ended inverter approved instead of an OTA in switched-capacitor integrator in (7). It is replaced by the self-biased fully differential super inverter to growth its noise rejection which complicates the common-mode feedback design (8). To improve the inverter's performance and reach low voltage, high speed and especially low power a self-biased digital inverter is presented in (9).

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By using the self-biasing technique, the digital inverter makes circuit to be less sensitive to process, supply voltage and temperature (PVT) and parameter variations. In this case, the switching currents can be greater than the quiescent bias current. Therefore, the external biasing voltage is unnecessary in this structure, and saving power and die area is supported. The approved self-biased digital inverter is proper to use in switched-capacitor circuits for low power, low voltage and high speed. As a prototype, a low power, low voltage switched-capacitor integrator based on a self-biased digital inverter is designed for practical applications.

This article is organized as follow: The operation principle of a self-biased digital inverter is described in section 2. The details of the architectural switched-capacitor integrator are discussed in section 3. Simulation results are shown in section 4, and the paper is concluded in section 5.

SELF_BIASED DIGITAL INVERTER CIRCUIT ARCHITECTURE

The self-biased digital inverter circuit is shown in Figure 1.

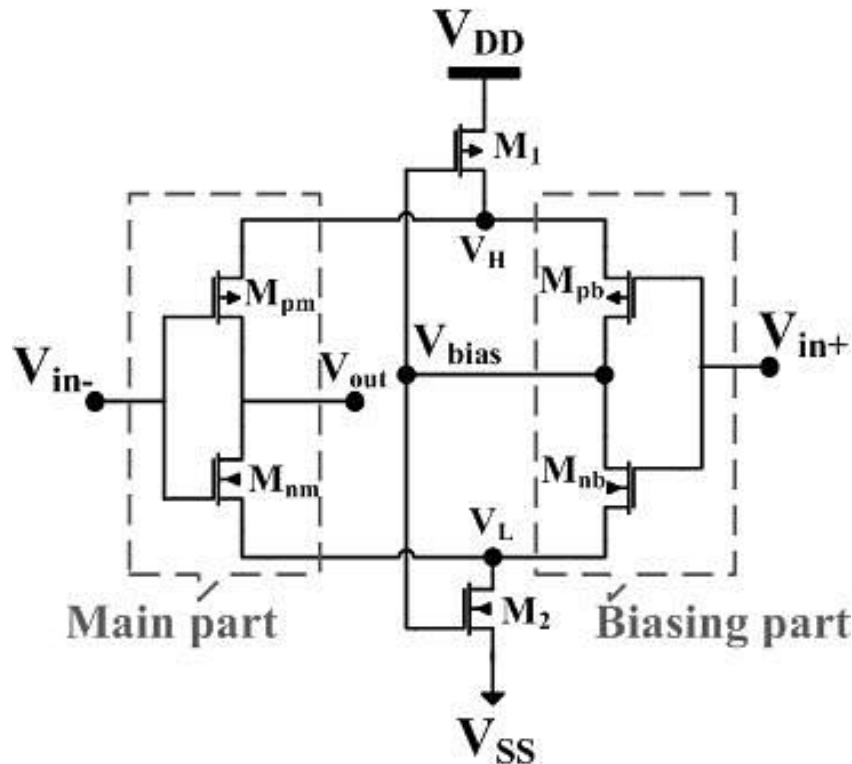


Figure 1. Self-biased digital inverter circuit

The self-biased digital inverter structure achieves excellent power efficiency and is compatible with terribly low voltage. In addition, in this structure supplying switching currents is bigger than the quiescent bias current that is one of the benefits for high speed and low power applications.

One necessary design aspect in this structure is the size of transistor and the region of biasing. Therefore, the transistors employed in main inverter and biasing inverter should be biased in linear region and are equally sized. M_1 and M_2 are used in the negative feedback loop in order to have a circuit that is compensate any PVT variation during circuit operation and stabilized the bias voltages. In this case, transistors M_1 and

M_2 are biased in triode mode. Therefore, the V_H and V_L can be set terribly near to supply voltages. These two voltages determine the output swing that might be very near to difference between the two supply rails (10), (11).

The differential-mode gain (A_{dm}) of the self-biased digital inverter is given by:

$$A_{dm} \cong \frac{g_{m1} + g_{m2}}{g_{out}} \quad (1)$$

Where g_{m1} and g_{m2} are the transconductances of transistors M_{pm-pb} and M_{nm-nb} , respectively and g_{out} is the output conductance of the self-biased digital inverter.

COMPLETE SWITCHED-CAPACITOR INTEGRATOR CIRCUIT

In modern technology, most analog integrated circuits make use of fully differential signal paths. By employing op-amps, this method results in differential outputs as well as inputs. Therefore, they are referred to as fully differential op-amps.

One disadvantage of using fully differential op-amps is adding a common mode feedback (CMFB) circuit to establish the Common mode output voltage. In the best case, CMFB will maintain Common mode voltage near to halfway

between the power supply voltages. Without this extra circuitry the Common mode voltage is left to drift. In feedback configuration mode, the common mode loop gain is not typically large enough to control its value (12). Hence, to solve this problem, the externally-biased operational amplifier is replaced by the self-biased digital inverter in the switched-capacitor integrator for low voltage, low power applications. The proposed switched-capacitor integrator architecture incorporating the self-biased digital inverter is shown in **Figure 2**.

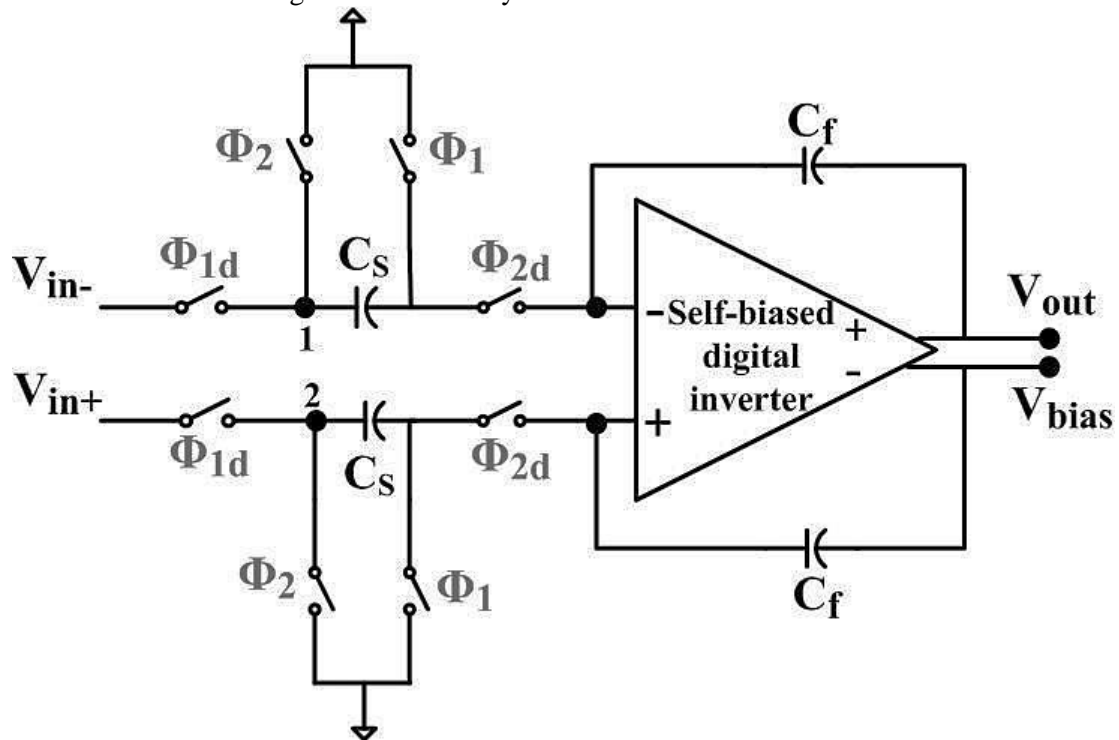


Figure 2. Switched-capacitor integrator architecture

To implement the proposed switched-capacitor integrator, non-overlap clocks with two phases required. Thus, integrator circuit works in two phases: sampling (Φ_1 & Φ_{1d}) and integration (Φ_2 & Φ_{2d}). During the sampling phase, the input signal is sampled in the sampling capacitor. The Φ_1 switch is turning off slightly earlier than Φ_{1d} to eliminate signal dependent charge injection in the sampling mode. In order to shift the floating potential to common-mode voltage level, Φ_2 is turning on slightly earlier than Φ_{2d} . once the Φ_{2d} switch is closed; the differential charges in sampling capacitors (C_s) are transferred to the feedback capacitors (C_f).

SIMULATION RESULTS

The proposed switched-capacitor integrator is implemented in a 90nm CMOS technology. The design specifications of the integrator are

summarized in **Table 1**. **Figure 3** shows the non-overlapping clock scheme. All utilized switches are NMOS only transistors. In order to ensure an adequately low switch resistance in a low supply voltage, the input voltage amplitude of the non-overlapping clock is set to 0.7V. The simulated voltage waveforms in the sampling phase at node 1 and node 2 in **Figure 2** are illustrated in **Figure 4 (a), (b)**, respectively. **Figure 5 (a), (b)** shows the voltage waveforms at the output of the integrator (node V_{out} and node V_{bias} in **Figure 2**) for $V_{dd}=0.7$ V. Compared to a switched-capacitor integrator incorporating the op-amps which consumes 3.4694mW of power (12), the power consumption in the proposed switched-capacitor integrator in this paper is only 1.9mW and the power consumption in the core of the proposed integrator is only 21nW. The performance of our integrator is compared with other switched-capacitor integrators in **Table 2**.

Table 1. Design specifications of the integrator

Technology	90nm CMOS	
Sampling Frequency	1.6 MHz	
Input Bandwidth	8KHz	
Sampling Capacitors (pF)	$C_{S1}=1000$	$C_{S2}=1000$
Feedback Capacitors (pF)	$C_{f1}=1$	$C_{f2}=1$

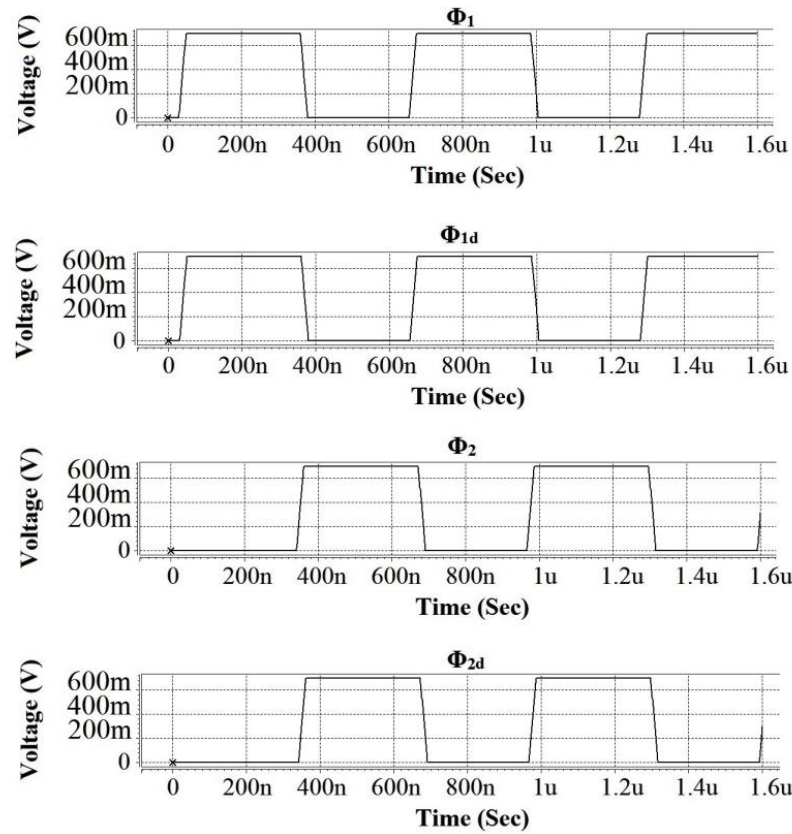


Figure 3. The non-overlapping clock scheme

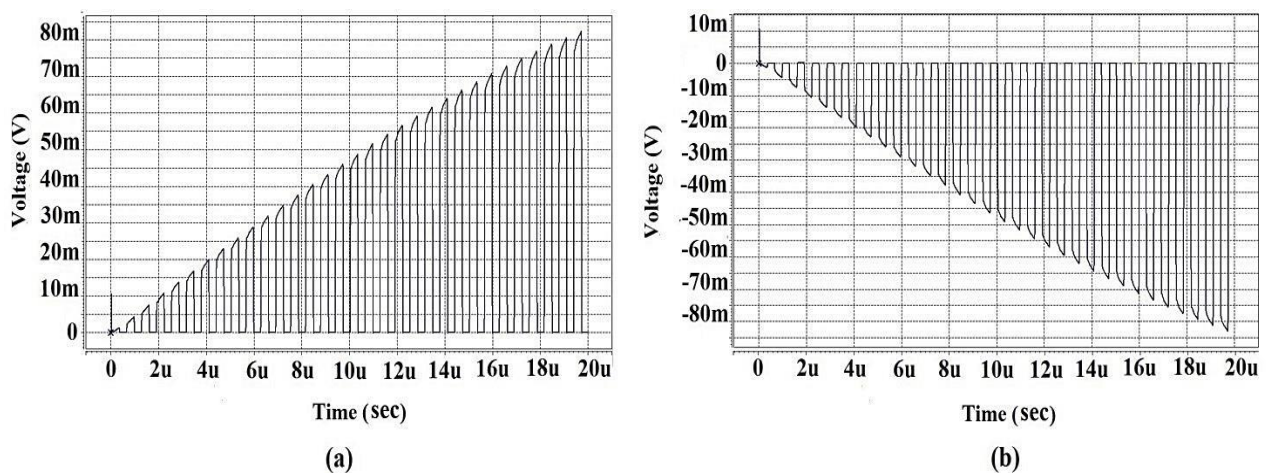


Figure 4. (a) Simulated voltage waveforms in the sampling phase at node 1 in Figure 2. (b) Simulated voltage waveforms in the sampling phase at node 2 in Figure 2.

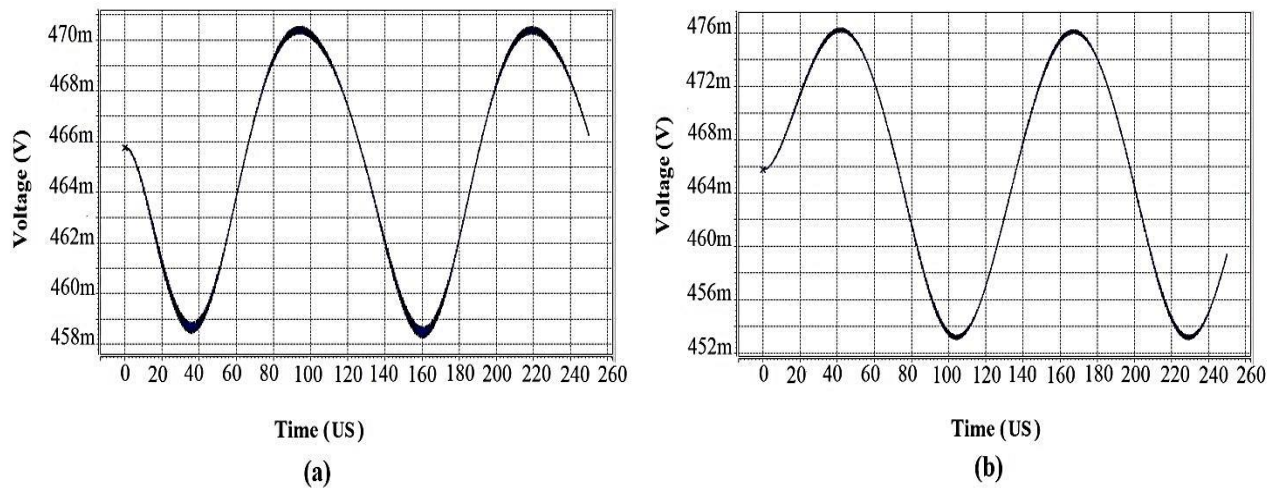


Figure 5. (a) Voltage waveforms at the output of the integrator node V_{out} in **Figure 2**. (b) Voltage waveforms at the output of the integrator node V_{bias} in **Figure 2**.

Table 2. Performance comparison of switched-capacitor integrators

Reference	Process (μm)	BW (KHz)	V_{dd} (V)	power (μW)
(3)	0.18	8	0.7	80
(5)	0.09	20	1	140
(6)	0.13	20	0.9	60
(8)	0.13	8	1.2	4.8
(9)	0.13	8	0.5	4
(12)	0.25	20	2.5	3469.4
This work	0.09	8	0.7	0.021

CONCLUSION

A 0.7-V 1.9mW switched-capacitor integrator based on a self-biased digital inverter is realized in this paper. The prototype switched-capacitor integrator employing the self-biasing technique has been designed in 90nm CMOS technology using only standard V_{TH} devices and consumes only 21nW of power in the core. The simulation results show that this integrator can be used for very low voltage and low power practical applications.

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